REMARKS

I. Status of the Claims

Applicants have amended claims 1, 2, 4, 6, 17, 19, 20, and 26, and added new claims 27 and 28. Applicants refer Examiner to paragraphs [0016], [0019], and [0026] for support for the new claims and claim amendments. Applicants believe that no new matter has been added by these claim amendments.

Claims 1-8, 10, 11, 13-20, and 26-28 are pending in this application. Claim 21 is withdrawn from consideration.

Applicants respectfully request reconsideration in view of these amendments and the following remarks and request examination of the new claims on the merits.

II. Rejections under 35 U.S.C. §103(a)

Claims 1-3, 15, 16, 18, and 26 stand rejected under § 103(a) as being unpatentable over U.S. Patent No. 6,632,729 to Paton ("Paton") in view U.S. Patent No. 6,909,151 to Hareland et al. ("Hareland"). Claims 1 and 26 are independent claims of this group, with claims 2, 3, 15, 16, and 18 depending directly or indirectly from claim 1. Applicants have amended claims 1, 2, and 26. Applicants respectfully traverse the rejections.

To begin with, Examiner misconstrues Applicants arguments (see Office Action page 11). Applicants argue that Paton's description of the oxide layer does not support the Examiner's stated reason to modify Paton. In particular, Examiner has failed to appreciate the facts as they are provided in both Paton and Hareland with regard to the oxide layer when formulating a rationale to modify Paton in view of Hareland.

Applicants remind Examiner that after consideration of all of the facts, Examiner must provide some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. (See M.P.E.P. §2142 III.) In an effort to satisfy this requirement, Examiner reasons that one skilled in the art would modify a substrate of Paton by placing a semiconductor body of Hareland on the substrate prior to depositing a high-k dielectric oxide layer on the substrate in order to modify device properties such as to enhance carrier mobility to improve device performance. (See Office

Action, page 5, last sentence.) Applicants submit that Examiner's stated reason fails to rationally follow from the facts and therefore fails to support a legal conclusion of obviousness.

Initially, with regard to the facts, Examiner correctly states that Paton does not explicitly disclose "a SiGe surface layer . . . on the substrate." (See Office Action page 3, middle of page.) Therefore, it is undisputed that Paton at least fails to describe any operation that could be construed as forming a SiGe surface layer on a silicon substrate as recited in the claims. Examiner relies on Hareland for disclosing forming a SiGe layer having an average Ge content less than about 10 at.% on the substrate. Hareland, however, does not disclose a device having an oxide layer between, for example, the gate dielectric layer 322 or gate dielectric layer 526 and an unreacted portion of a semiconductor body 308 or semiconductor film 508.

Examiner references Paton for disclosing the oxide layer according to the claimed invention. In this regard, Paton states that "when the substrate is a silicon (Si) or Si-containing substrate, a low-k silicon oxide layer, typically a SiO_2 layer, is formed at the interface between the semiconductor substrate and the high-k gate oxide layer." (See column 2, lines 40-44.) More importantly, Paton describes the presence of the SiO_2 layer at this location as being "disadvantageous" (see column 2, lines 42-44) and "deleterious" (see column 2, last line) to device performance, i.e., the SiO_2 layer increases the Effective Oxide Thickness. Paton describes a variety of semiconductor materials, both silicon containing and others, that are known to form the low-k SiO_2 layer. For example, the substrate may be a silicon substrate in the form of a single crystal, a polycrystal, or an amorphous form; a germanium substrate; a silicon-on-insulator substrate; or a silicon-germanium substrate. In addition, gallium arsenide substrates are also described. (See, for example, column 3, lines 51 to 57.) As set forth in Paton, a Laser Thermal Annealing process eliminates, or at least substantially reduces, oxygen out-diffusion from the high-k dielectric oxide layer during annealing and thus reduces or eliminates the low-k silicon oxide interfacial layer between the silicon substrate and the high-k gate oxide layer. In other words, Paton describes a process that improves device performance, i.e., a process that deactivates traps in the high-k gate oxide layer, by suppressing formation of a

deleterious low-k silicon oxide interfacial layer (see column 9, ll. 8–21) between the silicon substrate and the high-k gate oxide.

In contrast to Paton, Applicants claimed process comprises forming a SiGe surface layer on the silicon substrate and oxidizing a surface portion of the SiGe surface layer that substantially prevents oxidation of the silicon substrate during depositing or annealing. As is described in Applicants' specification, the oxide layer can contain SiO_2 and Ge diffusion away from the oxide can form a Ge-rich region at the oxide-SiGe surface layer interface. An annealing process can further homogenize the Ge distribution in the SiGe surface layer and form a SiO_2/SiGe interface with good structural and electrical properties. (See paragraph [0026] of the present application.)

In light of the facts from Paton and Hareland, Applicants submit that both Paton and Hareland fail to teach or suggest that forming a semiconductor device as claimed enhances carrier mobility or improves device performance in any way. Generally, neither reference indicates any advantage or performance benefit of any kind that would be associated with forming a SiGe surface layer on a silicon substrate as claimed. Further, rather than supporting a modification of Paton, the facts from Paton and Hareland would lead one skilled in the art away from the claimed invention because Paton describes a deleterious SiO_2 layer that forms on Si-containing substrates, e.g., SiGe substrates, during annealing. In essence, Paton describes improving device properties by reducing/eliminating formation of the interfacial SiO_2 layer on the Si-containing substrates. In spite of this, Examiner reasons that one skilled in the art would select SiGe having an average Ge content less than about 10 at.% from which to form a surface layer on a silicon substrate in order to improve device properties. Examiner, however, fails to address or provide any rationale as to why one skilled in the art would select SiGe in the first place. Applicants submit that no explanation is possible because Paton suggests that silicon substrates, including Si-Ge substrates, form a deleterious interfacial layer of low-k silicon oxide between the silicon substrate and the high-k gate oxide layer. Accordingly, one skilled in the art at the time of the invention would not reasonably expect to improve device properties by forming a layer of a known deleterious oxide-layer-forming material on a silicon substrate. In other words, one skilled in the art at the time of the invention

would not modify Paton in view of Hareland as Examiner suggests. Applicants submit therefore that Examiner's alleged modification of Paton amounts to picking and choosing using Applicants' claims and disclosure as a guide. Hindsight reasoning that includes knowledge gleaned only from Applicants' disclosure is not permitted during examination. (See M.P.E.P. §2145 X.A.)

Examiner has failed to establish a *prima facie* case of obviousness. Applicants believe that for at least these reasons amended claims 1 and claim 26 are nonobvious over Paton in view of Hareland. Applicants respectfully request withdrawal of the rejection.

Additionally, Applicants have amended claim 1 to recite that oxidizing a surface portion of the SiGe surface layer substantially prevents oxidation of the silicon substrate during depositing of the high-k dielectric layer or during the annealing process. Applicants have amended claim 26 to recite depositing an oxygen-containing high-k dielectric layer on the SiGe surface layer and forming an oxide layer by diffusing oxygen from the oxygen-containing high-k dielectric layer or by exposing the SiGe surface layer to an oxidizing gas under oxidizing conditions, wherein oxidizing the SiGe surface layer substantially prevents oxidation of the silicon substrate. As is noted above, unlike the Applicants' claimed invention where oxidation of the substrate is substantially prevented, Paton clearly describes oxidation of silicon substrates by diffusion of oxygen from the high-k gate dielectric oxide layer during annealing. Hareland does not cure the deficiency of Paton because Hareland does not address or imply oxidation of the semiconductor bodies. Therefore, for at least these additional reasons, amended claims 1 and 26 are nonobvious over Paton in view of Hareland.

Since claims 2, 3, 15, 16, and 18 depend from amended claim 1, Applicants submit that these claims are also patentable for at least the same reasons discussed in Applicants' preceding remarks.

Claims 4-8 stand rejected under § 103(a) as being unpatentable over Paton in view of Hareland and in view of EP 0684 650 B1 to Hiroshi et al. ("Hiroshi"). Claims 4-8 depend directly or indirectly from amended claim 1. Applicants have amended claim 4 to recite the Si substrate according to the amendments of claim 1. Applicants

respectfully request that the rejections be withdrawn. The arguments presented above for amended claims 1 and 26 apply equally to this rejection. As set forth above, Paton in view of Hareland does not teach or suggest the invention claimed in amended claim 1. Hiroshi does not cure that deficiency. Accordingly, amended claim 4 and claims 5-8 are nonobvious over Paton in view of Hareland in further view of Hiroshi. Thus, withdrawal of the rejections is respectfully requested.

Claims 10 and 11 stand rejected under § 103(a) as being unpatentable over Paton in view of Hareland and U.S. Patent Application Publication No. 2003/0218189 to Christiansen et al. ("Christiansen"). Claims 10 and 11 depend directly from amended claim 1. The arguments presented above for amended claims 1 and 26 apply equally to this rejection. As set forth above, the combination of Paton in view of Hareland does not teach or suggest the invention claimed in amended claims 1 and 26. Christiansen does not cure that deficiency. Claims 10 and 11 are nonobvious over Paton in view of Hareland in further view of Christiansen. Thus, withdrawal of the rejection of claims 10 and 11 is respectfully requested.

Claims 13-14 and 19-20 stand rejected under § 103(a) as being unpatentable over Paton in view of Hareland and in further view of Westlinder et al., *Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-k dielectric,* European Solid-State Device Research, September 2003, pp. 525-528 ("Westlinder"). Claims 13, 14, and 19 depend directly from amended claim 1. Claim 20 is an independent claim. Applicants have amended claims 19 and 20. Applicants respectfully request withdrawal of the rejection.

Applicants note that Examiner did not respond to the substance of Applicants' arguments over Examiner's combination of Paton in view of Hareland in further view of Westlinder. Applicants submit that Paton in view of Hareland and in further view of Westlinder fails to teach or suggest the inventions of claims 13 and 14, and amended claims 19 and 20. The arguments presented above for amended claims 1 and 26 apply equally to the rejection of claims 13, 14, 19, and 20. Westlinder fails to cure what Paton in view of Hareland is missing. Consequently, claims 13 and 14 and amended claims 19 and 20 are nonobvious over this combination of references.

Applicants have amended claim 19 to recite exposing the SiGe surface layer to the oxygen-containing gas, which is consistent with Applicants' specification and the method recited in amended claim 1. Additionally, Applicants have amended claim 20 to recite that oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the silicon substrate during the depositing or the annealing. As set forth above with regard to the rejections of claims 1 and 26, Paton clearly describes oxidation of silicon substrates by diffusion of oxygen from the high-k gate dielectric oxide layer during annealing. Hareland does not cure the deficiency of Paton, because Hareland does not address or imply oxidation of the semiconductor bodies. For at least these additional reasons, amended claim 20 is nonobvious over Paton in view of Hareland and in further view of Westlinder.

Claim 17 is rejected under § 103(a) as being unpatentable over Paton in view of Hareland and U.S. Patent No. 5,259,881 to Edwards et al. ("Edwards"). Claim 17 depends directly from amended claim 1. Applicants have amended claim 17 to provide antecedent basis for the Si substrate recited in amended claim 1. Applicants respectfully traverse the rejection. The arguments presented above for amended claims 1 and 26 apply equally to this rejection, the combination of Paton in view of Hareland does not teach or suggest the invention claimed in amended claim 1. Edwards does not cure this deficiency. Amended claim 17 is nonobvious over Paton in view of Hareland and Edwards. Thus, withdrawal of the rejection of claim 17 is respectfully requested.

New claims 27 and 28 each depend directly from amended claim 26. Claim 27 recites that oxidizing the surface portion of the SiGe surface layer includes exposing the surface portion to an oxidizing gas under oxidizing conditions. Claim 28 recites that oxidizing the surface portion of the SiGe surface layer includes diffusing oxygen from the oxygen-containing high-k dielectric layer into the surface portion. As set forth above with regard to the rejection of amended claims 20 and 26, none of Paton, Hareland, or Westlinder teach oxidizing a SiGe surface layer between a high-k dielectric layer and a silicon substrate by exposing the SiGe surface layer to oxidizing conditions or by diffusing oxygen from the oxygen-containing high-k dielectric layer. For at least these reasons, Applicants submit that new claims 27 and 28 are nonobvious over Paton in view

of Hareland or over Paton in view of Hareland in further view of Westlinder. Applicants request allowance of these claims.

III. Conclusion

In view of the foregoing amendments to the claims, new claims, and remarks given herein, Applicants respectfully believe this case is in condition for allowance and respectfully request allowance of the pending claims. If the Examiner believes any detailed language of the claims requires further discussion, the Examiner is respectfully asked to telephone the undersigned attorney so that the matter may be promptly resolved. The Examiner's prompt attention to this matter is appreciated.

This response is believed to be timely filed within the shortened statutory three-month period, as March 1st fell on a Sunday and this response is filed on Monday, March 2, 2009. Applicants are of the opinion that no fee is due as a result of this Amendment. If any charges or credits are necessary to complete this communication, please apply them to Deposit Account No. 23-3000.

Respectfully submitted,

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